Imperial College London

Lecture 12

Analogue-to-Digital Conversion

Peter Cheung
Department of Electrical & Electronic Engineering
Imperial College London

URL: www.ee.imperial.ac.uk/pcheung/teaching/E2_CAS/
E-mail: p.cheung@imperial.ac.uk

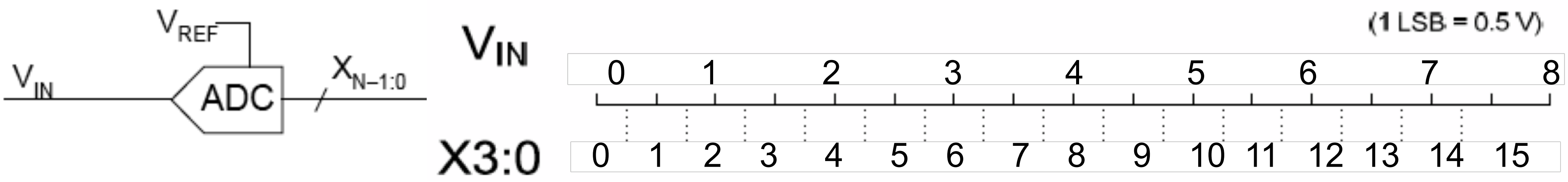
Lecture Objectives

- Understand the relationship between the continuous input signal to an Analog-to-Digital converter and its discrete output
- Understand the source and magnitude of quantisation noise
- Understand how a flash converter works
- Understand the principles behind a successive approximation converter
- Understand how a successive approximation converter can be implemented using a state machine
- Understand the need for using a sample/hold circuit with a successive approximation converter

References:

- "Data Converter Architectures" in Data Conversion Handbook by Analog Devices

Analogue to Digital Conversion



- Converters with only +ve input voltages are called ***unibipolar*** converters and usually round (V_{IN} ÷ 1LSB) to the ***nearest*** integer.

$$X = \text{round}\left(\frac{V_{IN}}{1\ \text{LSB}}\right)$$

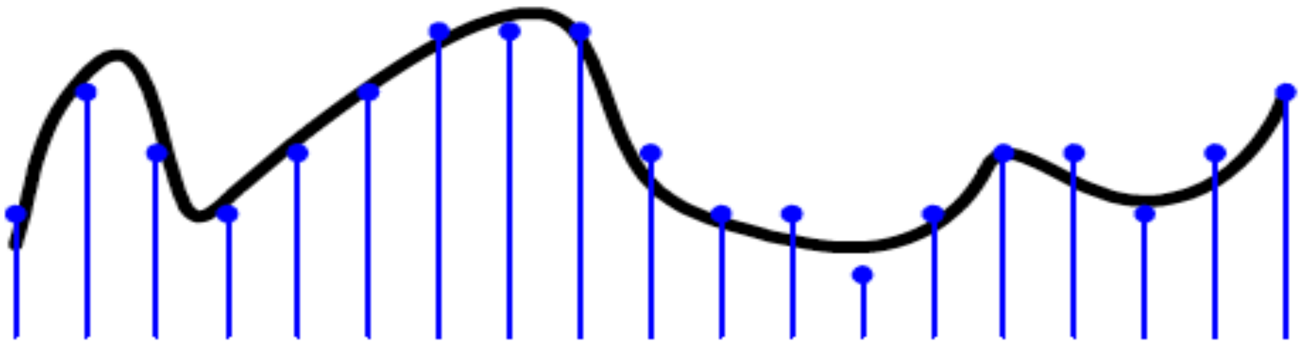
- Example:
  - If 1 LSB = 0.5 V, then V_{IN} = 2.8 V will be converted to:

$$X = \text{round}\left(\frac{2.8}{0.5}\right) = \text{round}(5.6) = 6$$

> Analog to digital conversion **destroys information**: we convert a range of input voltages to a single digital value.

Sampling

- To process a continuous signal in a computer or other digital system, you must first sample it:



Time Quantisation

- Samples taken (almost always) at regular intervals: sample frequency of f_{samp}.
- This causes *aliasing*: A frequency of f is indistinguishable from frequencies $k\, f_{samp} \pm f$ for all integers k.
- No information lost if signal contains only frequencies below $\frac{1}{2} f_{samp}$. This is the *Nyquist limit*.

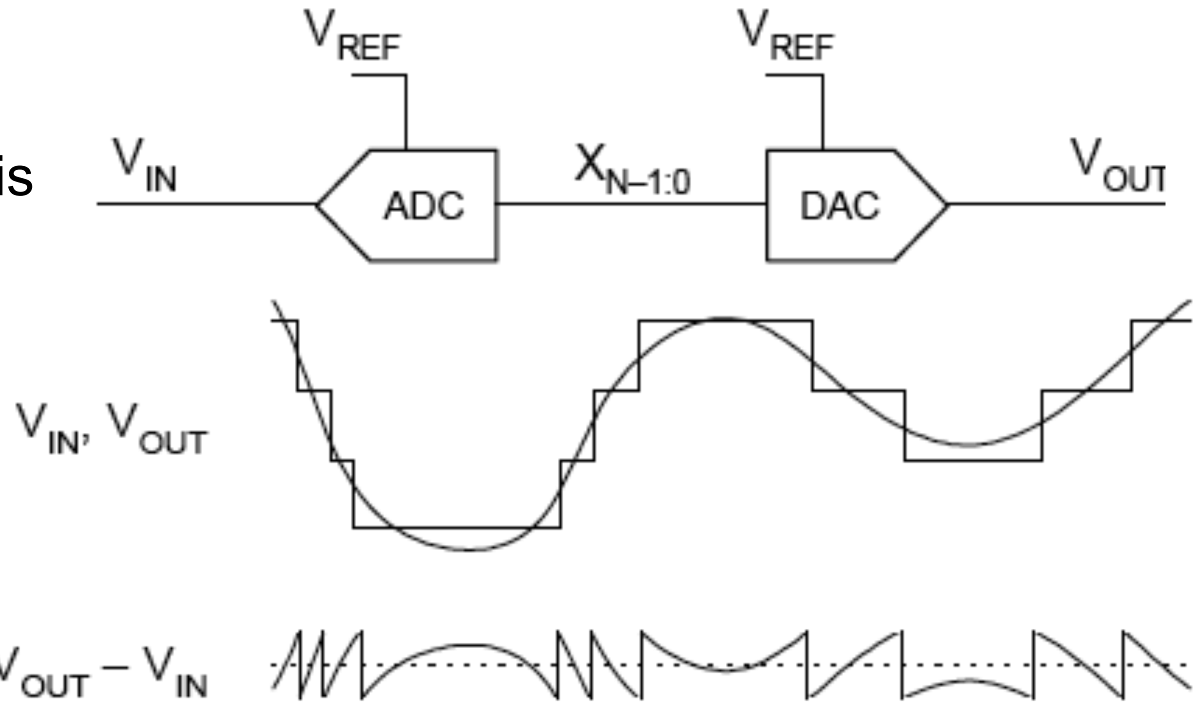
Amplitude Quantisation

- Amplitude of each sample can only take one of a finite number of different values.
- This adds quantisation noise: an irreversible corruption of the signal.
- For low amplitude signals it also adds distortion. This can be eliminated by adding dither before sampling.

Quantisation Noise

- *VOUT* is restricted to discrete levels so cannot follow VIN exactly. The error, *VOUT – VIN* is the quantisation noise and has an amplitude of ± ½ LSB.
- If all error values are equally likely, the RMS value of the quantisation noise is:

$$\sqrt{\int_{-\frac{1}{2}}^{+\frac{1}{2}} x^2 dx} = \frac{1}{\sqrt{12}} = 0.3 \text{ LSB}$$

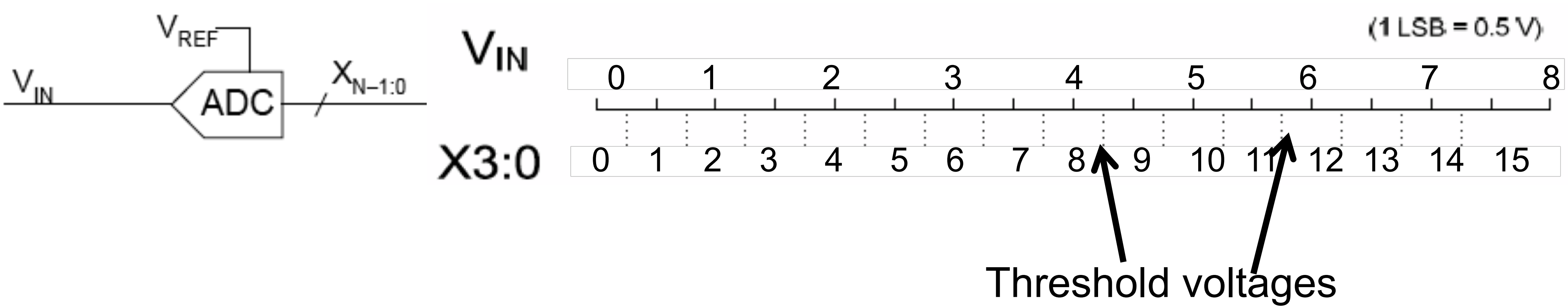


Signal-to-Noise Ratio (SNR) for an n-bit converter

- Ratio of the maximum sine wave level to the noise level:
  - Maximum sine wave has an amplitude of $\pm 2^{n-1}$ which equals an RMS value of $0.71 \times 2^{n-1} = 0.35 \times 2^n$.
  - SNR is:

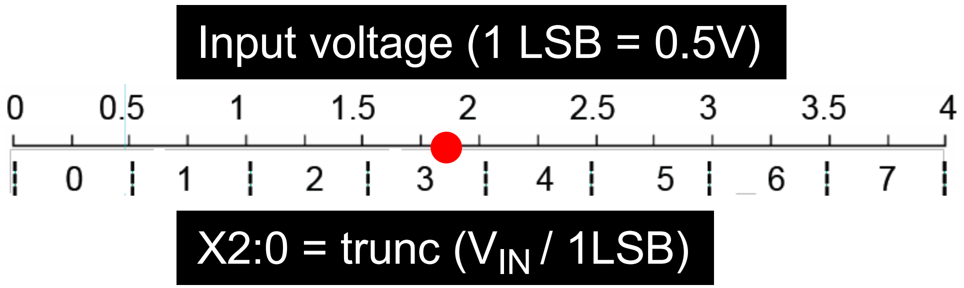
$$20\log_{10}\left(\frac{0.35 \times 2^n}{0.3}\right) = 20\log_{10}(1.2 \times 2^n) = 1.8 + 6n \text{ dB}$$

Threshold Voltages

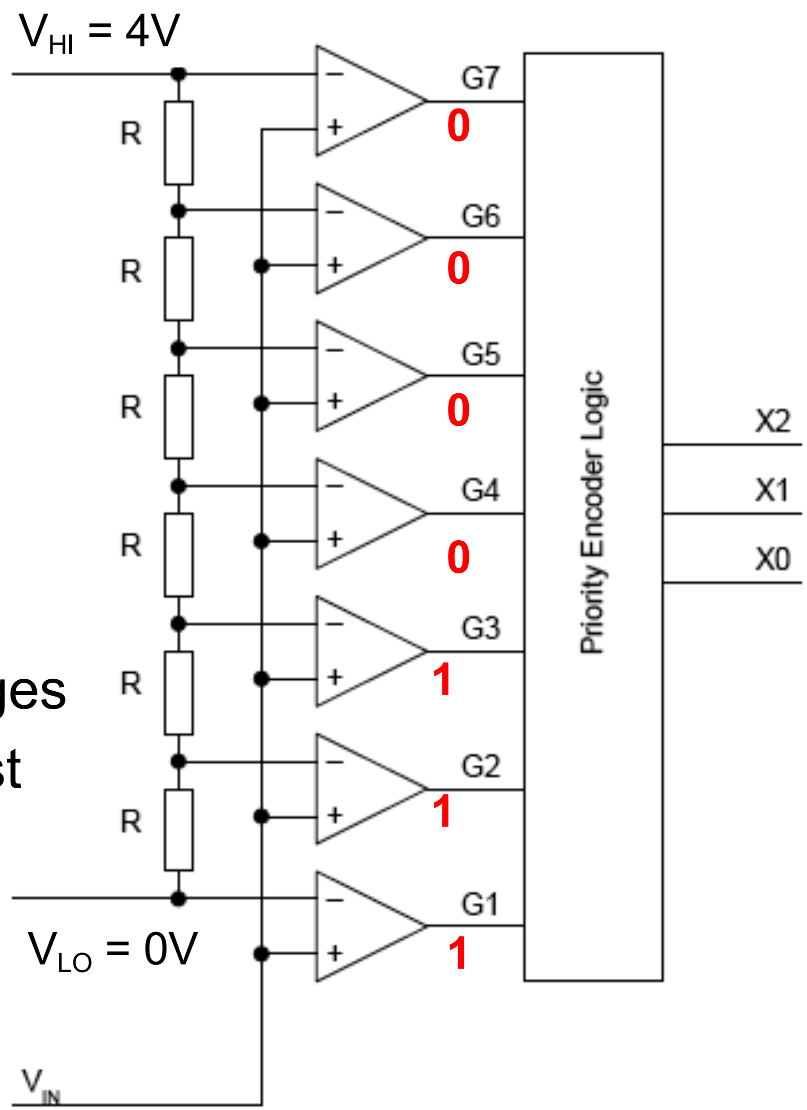


- Each value of X corresponds to a range of values of V_{IN}.
- The voltage at which V_{IN} switches from one value of X to the next is called a ***threshold voltage***.
- The task of an A/D converter is to discover which of the voltage ranges V_{IN} belongs to. To do this, the converter must compare V_{IN} with the threshold voltages.
- The threshold voltages corresponding to X are at (X±½) LSB

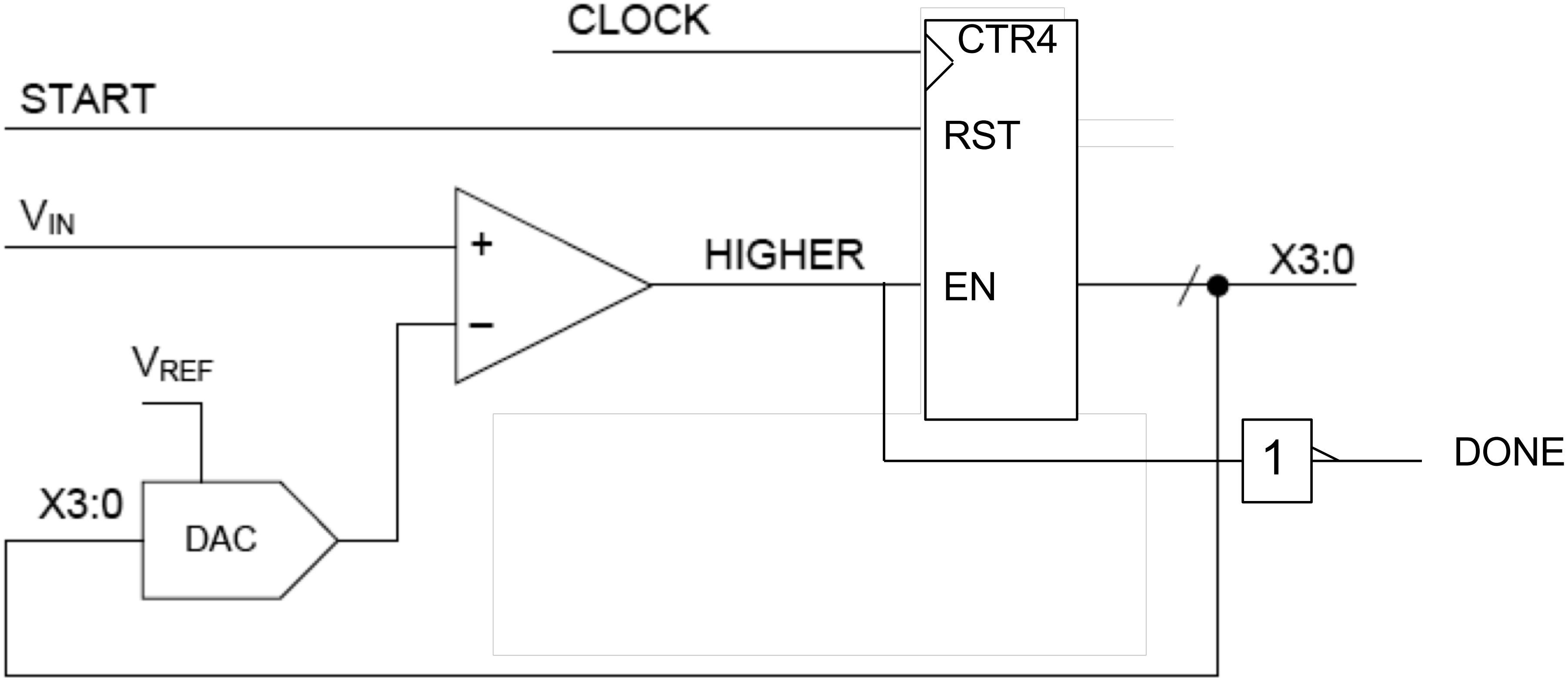
Flash A/D Converter



- For an n-bit converter we have 2^n-1 ***threshold voltages***
- Use 2^n-1 comparators:
- Resistor chain used to generate threshold voltages
- Priority encoder logic must determine the highest G_n input that equals 1.
- 12-bit converter needs 4095 comparators on a single chip!
- This example shows a unipolar converter

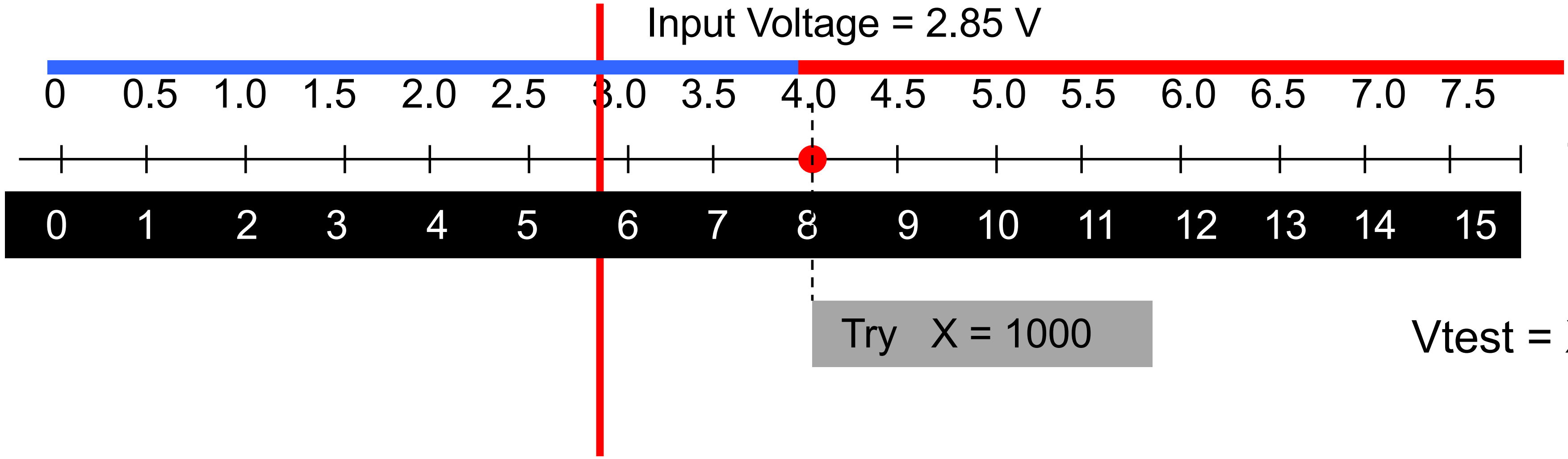


A Naïve ADC using a counter



- Here is a simple ADC using a DAC, a comparator and a binary up counter.

Successive Approximation ADC (1)



4-bit converter

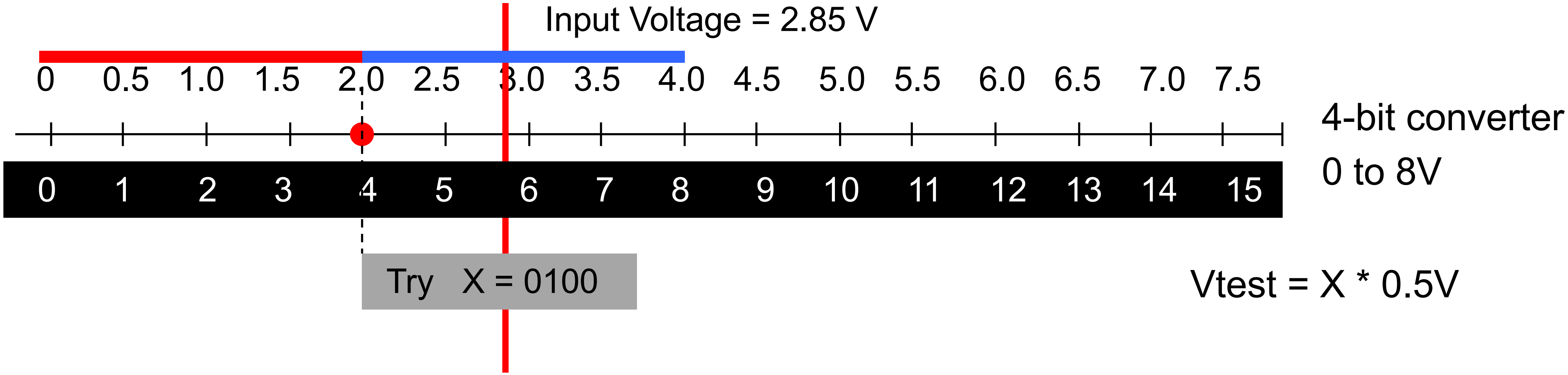
0 to 8V

Vtest = X * 0.5V

- First guess: set MSB to 1
- Set test voltage to 4V
- Is input ≥ 4V?
- If input ≥ 4V, X = 1???, keep MSB

  else X = 0???, clear MSB

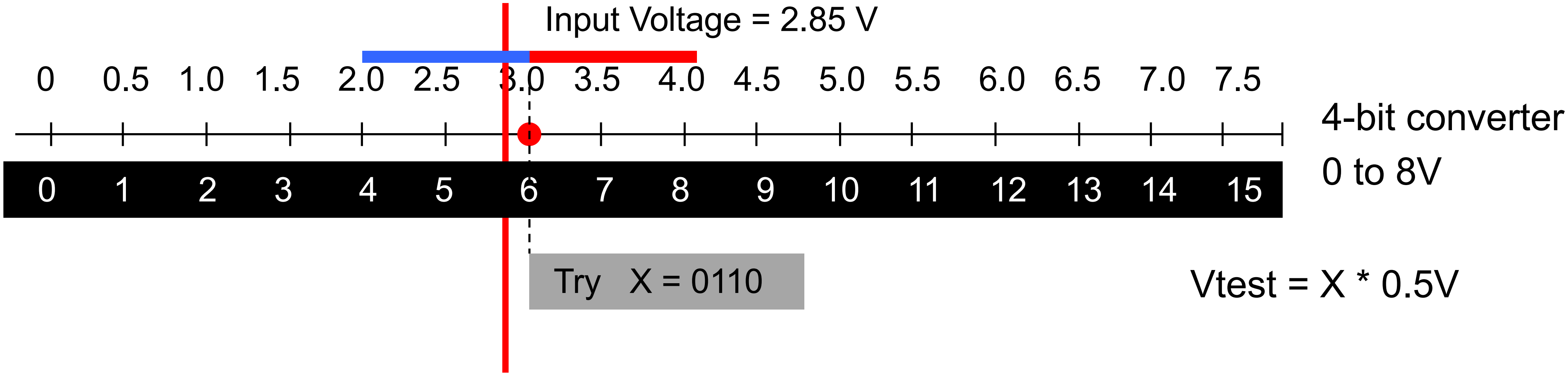
Successive Approximation ADC (2)



- Second guess: set next bit to 1 (X = 0100)
- Set test voltage to 2V
- Is input ≥ 2V?
- **If input ≥ 2V, X = 01??, keep bit as 1**

  else X = 00??, clear bit to 0

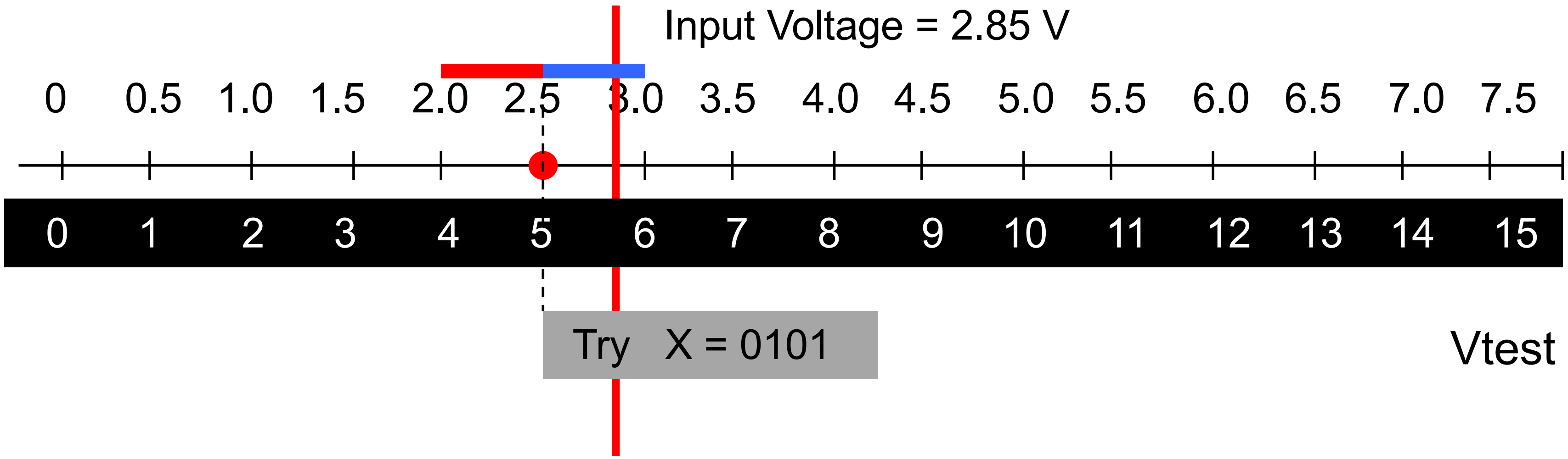
Successive Approximation ADC (3)



- Third guess: set next bit to 1 (X = 0110)
- Set test voltage to 3V
- Is input ≥ 3V?
- If input ≥ 3V, X = 011?, keep bit as 1

  else X = 010?, clear bit to 0

Successive Approximation ADC (4)



4-bit converter

0 to 8V

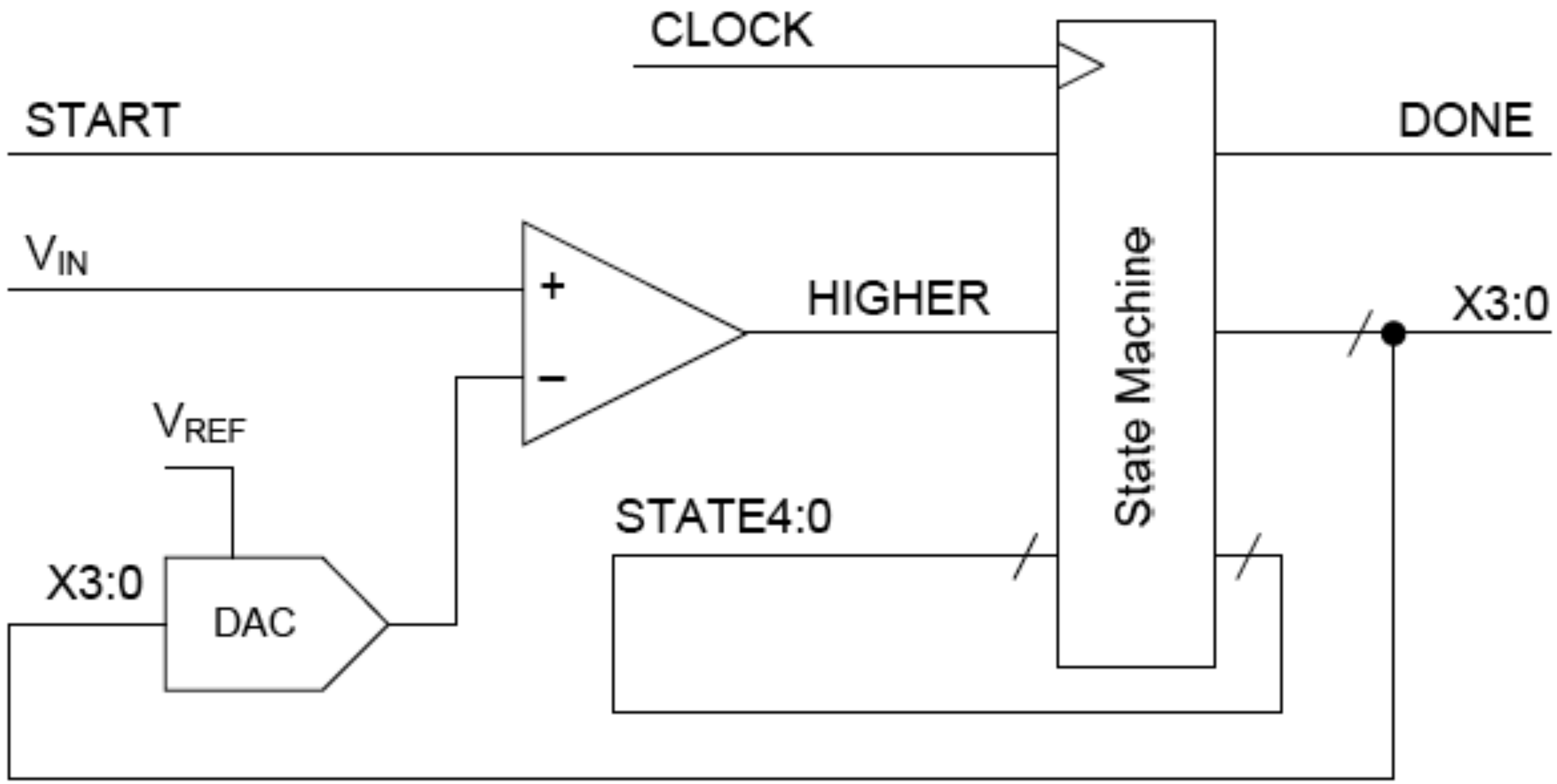
Vtest = X * 0.5V

- Fourth guess: set next bit to 1 (X = 0101)
- Set test voltage to 2.5V
- Is input ≥ 2.5V?
- **If input ≥ 2.5V, X = 0101, keep bit as 1**

  else X = 0100, clear bit to 0

- Make successive guesses and use a comparator to tell whether your guess is too high or too low.
- Each guess determines one bit of the answer and cuts the number of remaining possibilities in half.

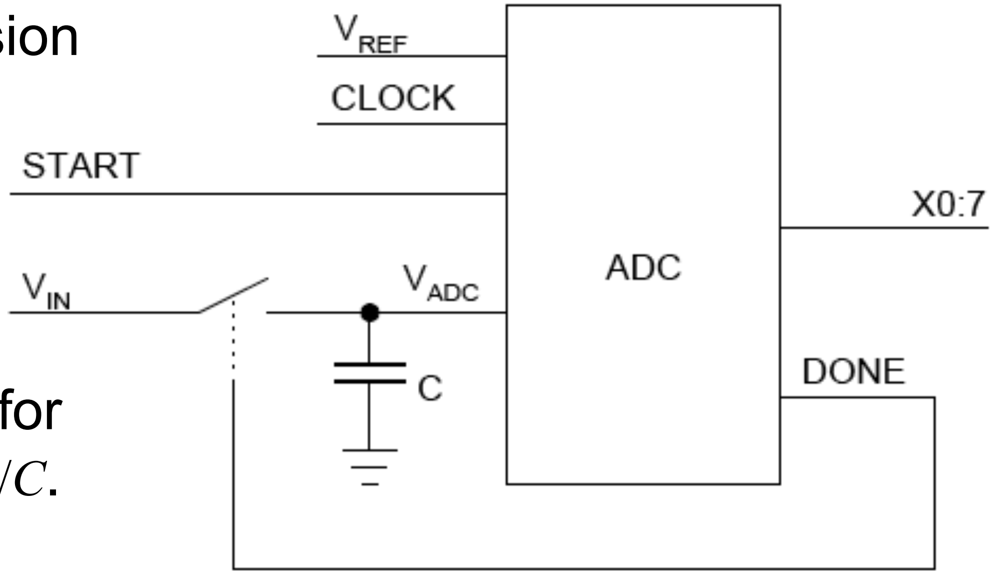
Successive Approximation ADC (5)

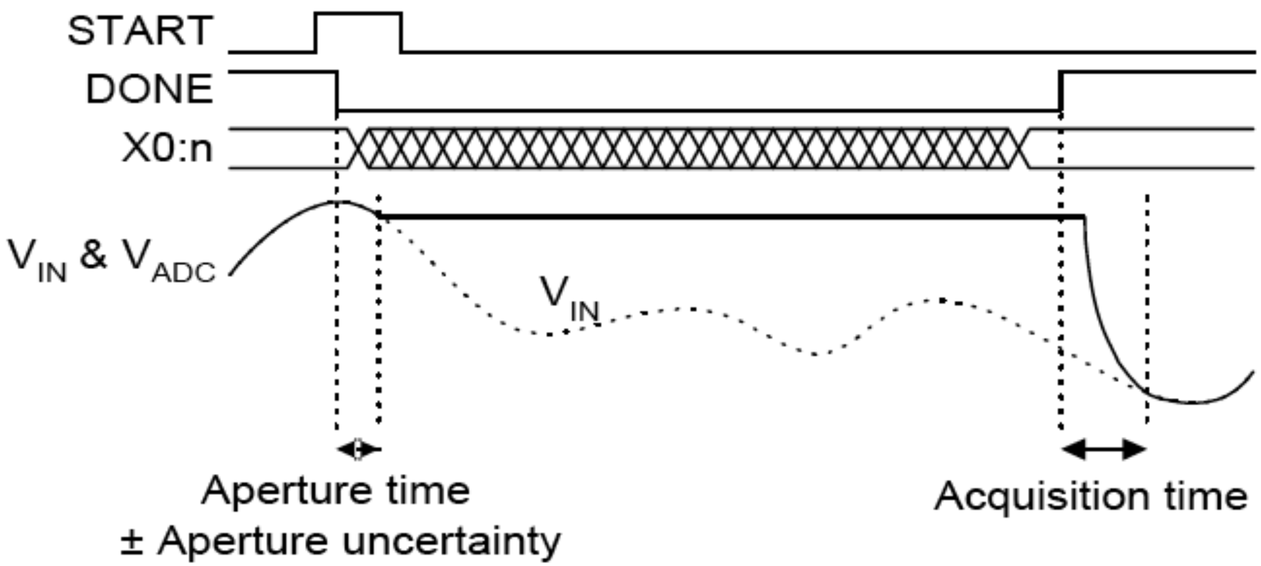


- Use a DAC to generate the threshold voltages and a state machine to create the sequence of guesses
- A DAC input of n generates the threshold between n–1 and n which equals (n–½) × 1 LSB

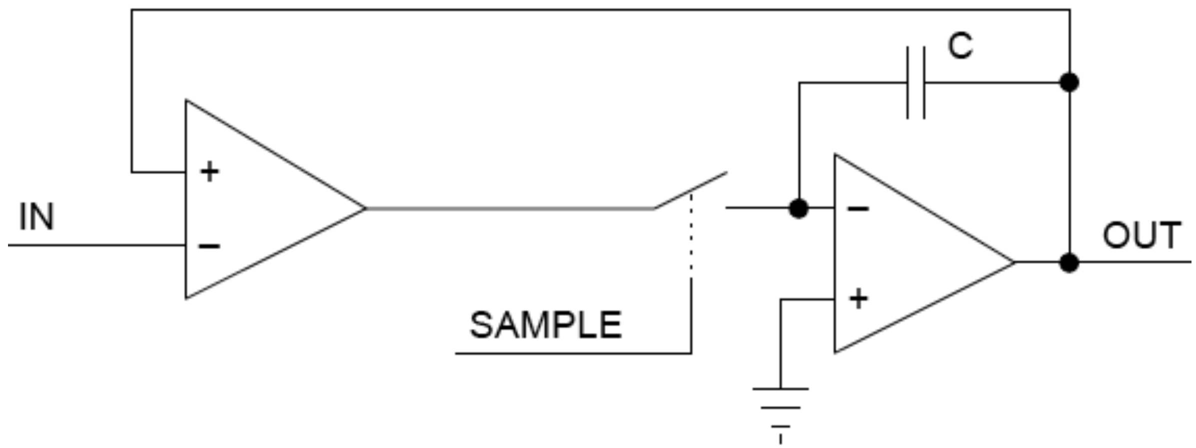
A/D conversion with sample/hold

- Input switch is opened during the conversion so V_{ADC} remains constant (HOLD).
- Choice of C is a compromise:
  - Big C keeps constant voltage despite leakage currents since $dV/dt = I_{leakage}/C$
  - Small C allows faster acquisition time for any given input current since $dV/dt = I_{in}/C$.





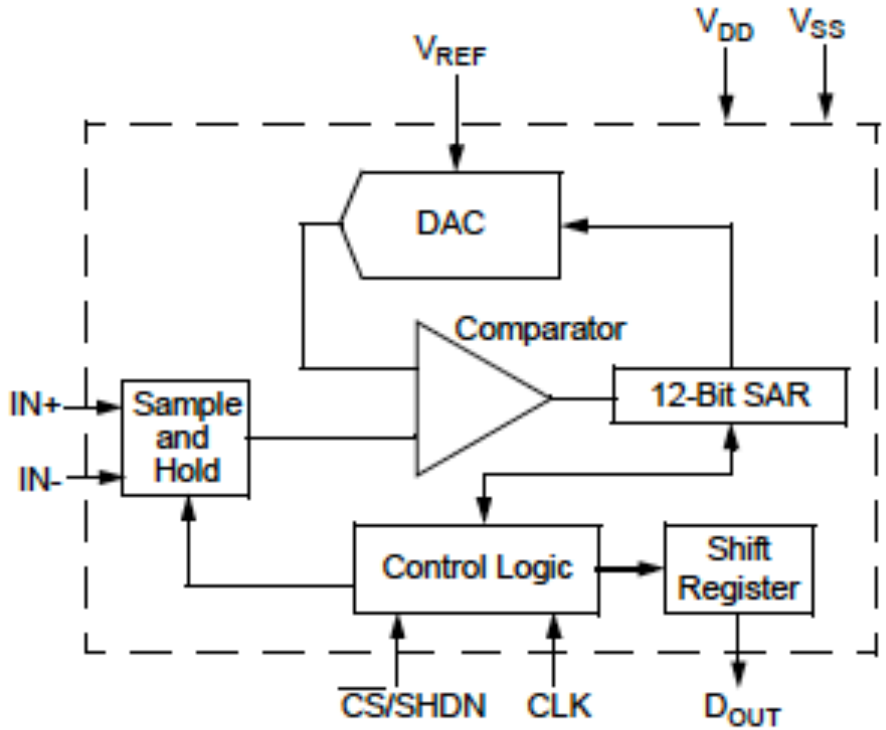
Sample/Hold Circuit



- When switch is open:
  - Leakage currents through open switch and op-amp input will cause output voltage to drift up or down.
  - Choose capacitor large enough that this drift amounts to less than 0.5 LSB during the time for a conversion
  - Converters with high resolution or long conversion times need larger capacitors
- When switch closes:
  - Charge rate of capacitor is limited by the maximum op-amp output current. This determines the ***acquisition time***: to acquire the signal to within ½LSB. It is typically of the same order as the conversion time.
- Value of C is a compromise: big C gives slow acquisition, small C gives too much drift.

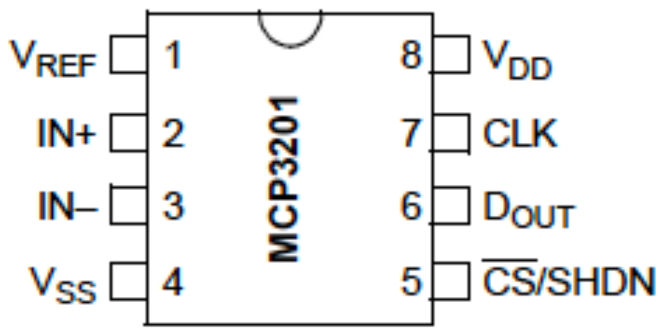
ADC used in Lab

- **Microchip MCP3201** 12-bit ADC
- Uses **successive approximation** architecture
- Serial Peripheral Interface (SPI)



Features

- 12-Bit Resolution
- ±1 LSB max DNL
- ±1 LSB max INL (MCP3201-B)
- ±2 LSB max INL (MCP3201-C)
- On-chip Sample and Hold
- SPI Serial Interface (modes 0,0 and 1,1)
- Single Supply Operation: 2.7V - 5.5V
- 100 ksps Maximum Sampling Rate at V_{DD} = 5V
- 50 ksps Maximum Sampling Rate at V_{DD} = 2.7V



Other types of Converter

Sampling ADC

- Many A/D converters include a sample/hold within them: these are ***sampling*** A/D converters.

Oversampling DAC and ADC

- ***Oversampling*** converters (also known as sigma-delta $\Sigma\Delta$ or delta-sigma $\Delta\Sigma$ converters) sample the input signal many times for each output sample. By combining digital averaging with an error feedback circuit they can obtain up to 20 bits of precision without requiring a high accuracy resistor network (hence cheaper). A typical oversampling ratio is 128X, i.e. the input is sampled at 6.4MHz to give output samples at 50 kHz. Most CD players use an oversampling DAC.